PRINTED WIRING BOARD MANUFACTURING TECHNOLOGY CENTER

PROBLEM / OBJECTIVE

In July of 1998, the Printed Wiring Board (PWB) industry approached congress for the initiation of a center to address lack of U.S. research and development in board technology. The PWB Manufacturing Technology Center (PMTEC) was then formed to address the development of state-of-the-art PWB technology. PMTEC worked to ensure an affordable, responsive, and reliable U.S. PWB manufacturing capability to meet current and future DoD requirements. The effort was executed through an integrated program of research, education, and technology transfer. PMTEC focused on propelling forward the development of bare board technology such that it supported current and future advances in the semiconductor packaging/printed wiring assembly technology. The effort also addressed unique and critical military PWB needs, such as the ability to withstand harsh environments, long-term availability and reliability, rapid insertions, and integration of new technology.

ACCOMPLISHMENTS / PAYOFF

Projects: PMTEC successfully teamed with the PWB industry and defense-related companies to initiate several efforts to impact DoD weapon systems and commercial products. Eighteen projects have been completed through the center:

- PWB Micro-Packaging for Missile Health Assessment Phase I & Phase II
- Interconnect Stress Testing (IST) of PWBs
- Low Cost High Frequency Laminate Modeling & Design
- Next Generation Photolithography
- Lead Free Solders/Surfaces for PWBs
- Reliability of Chip Carrier Substrates
- Microvia Registration Reliability
- Microvia Demonstration for GMLRS-SAASM
- Accelerometer on Laminate
- Development of Liquid Crystal Polymer (LCP) Near Hermetic Packing
- Vacuum Sealer for Package Development
- Spectrometer Development for UGV
- Laminate integration of MEOMS sensors
- Power Chip on Board Phase I & II
- Next Generation Avionics Electronics for THAAD
- Alabama A&M Prototype PWB Manufacturing

Potential cost avoidance:

- $14.1M for Comanche and $11.1M for F-22 (Power Chip-on-board technology to be implemented in Spring 2003)
- $36.7M for DoD-wide GPS/ Guided Multiple Launch Rocket System (GMLRS) SAASM programs Estimated $250savings per unit, based on 146,800 units over 5 years (Microvia Substrate Demo of Security Modules ended in Phase1; unfunded Phase 2-implementation).
- Reduced manufacturing costs of boards for Joint Tactical Information Distribution System (JTIDS), Army Tactical Missile Systems (ATACMS),
  (Next Generation Photolithography System; implemented in Rockwell Collins facility).
- $61M projected cost avoidance for 18 projects over 5 years.

TIMELINE

Start Date: July 1998
End Date: March 2003

FUNDING

Total: $7.500M
Cost Sharing/Leveraging: $2.500M

PARTICIPANTS

Auburn University	Alabama A&M University
Anvik	Boeing
Celestica	CCI
Excellon	Hadco
Foster Miller	IIT Research Institute(IITRI)
IPC	Johnson-Matthey
Lockheed Martin	Merix Morton
Morgan Research	Tyco

Florida International University
Interconnect Technology Research Institute (ITRI)

Morgan Research	Multitek
Northrop Grumman	Praegitzer

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PWB Solutions	Raytheon
Rockwell Collins	Sandia